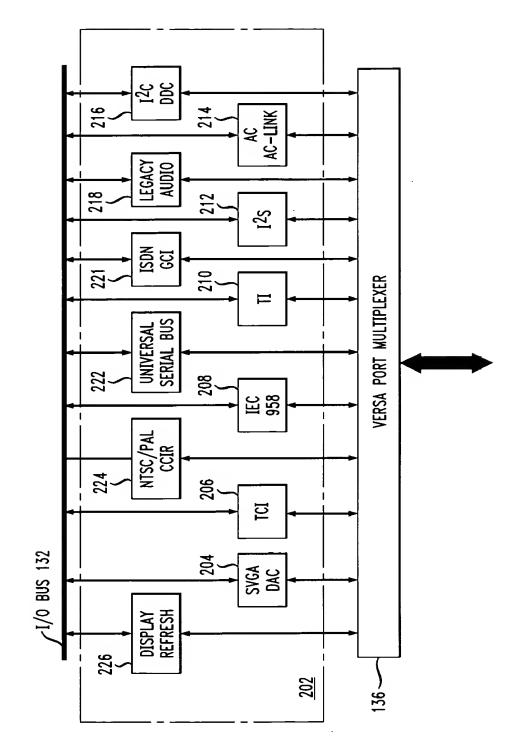
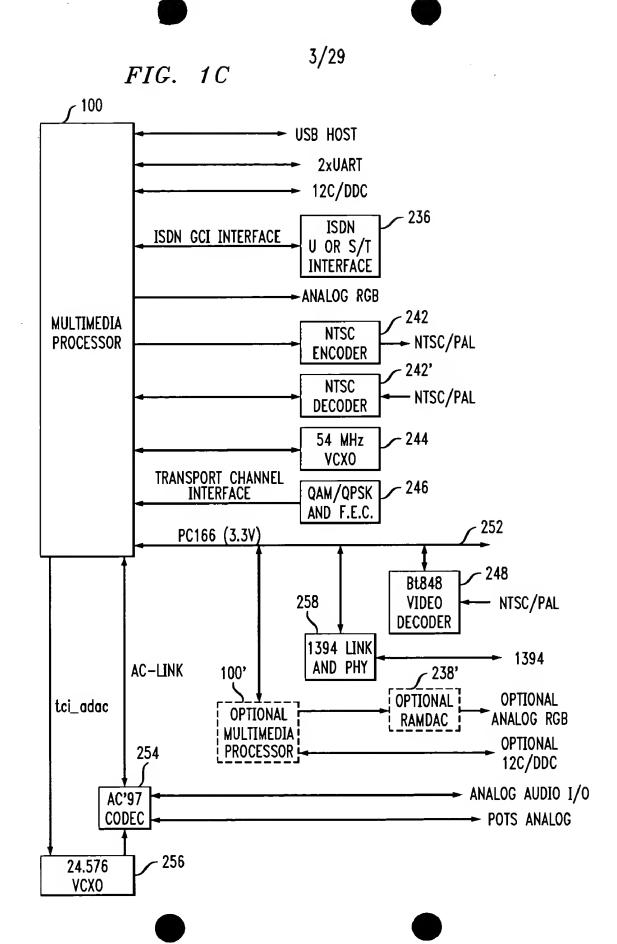
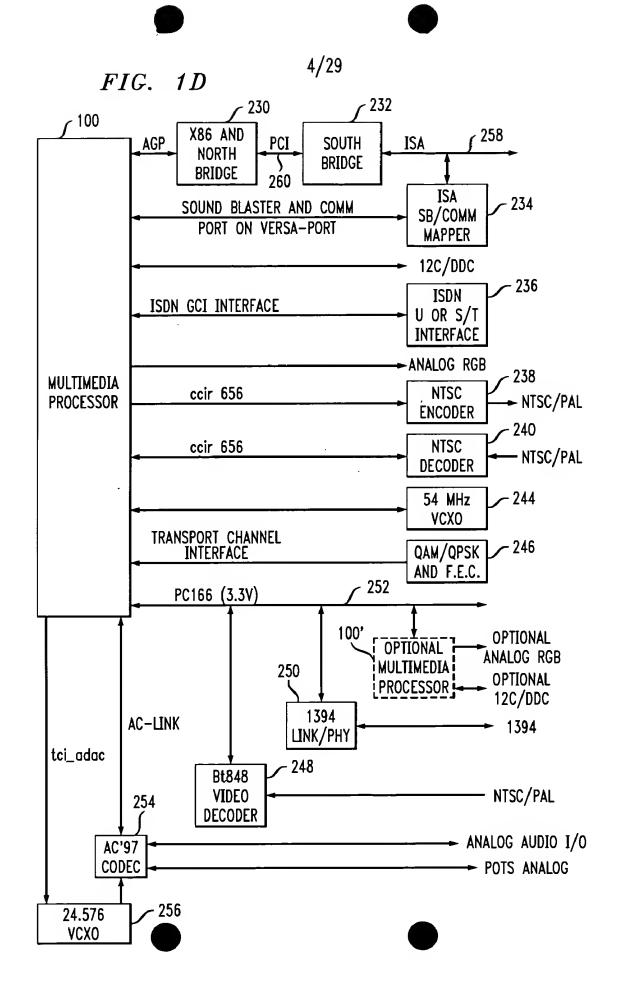
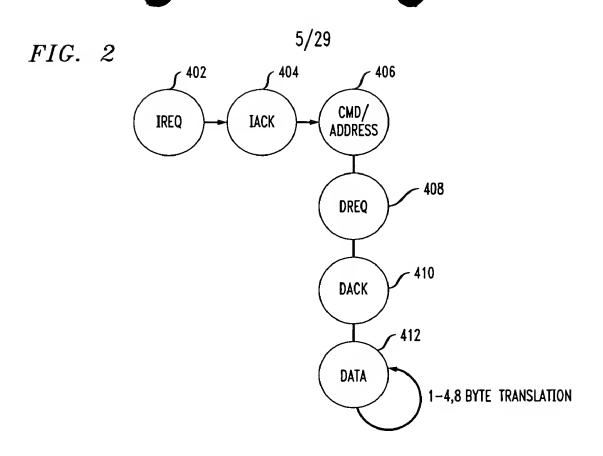


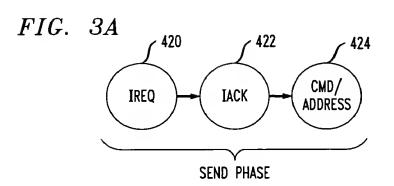
FIG. 1B

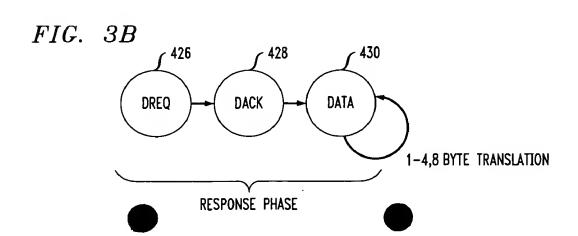












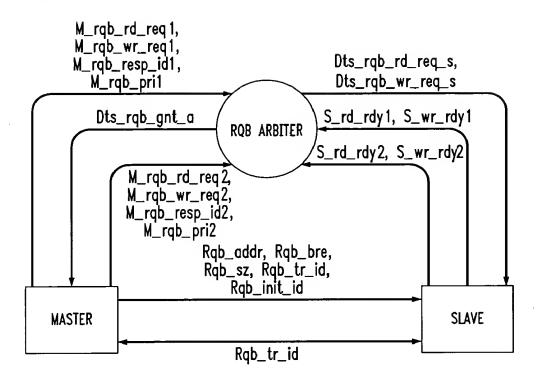


FIG. 4B

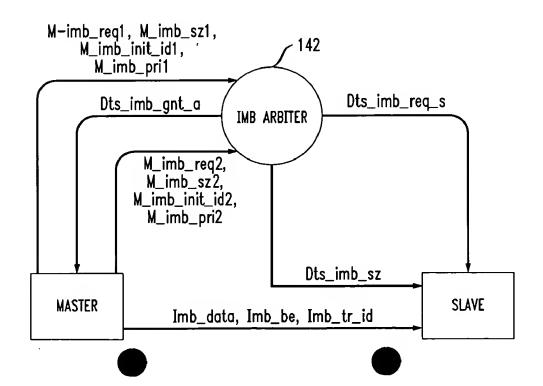
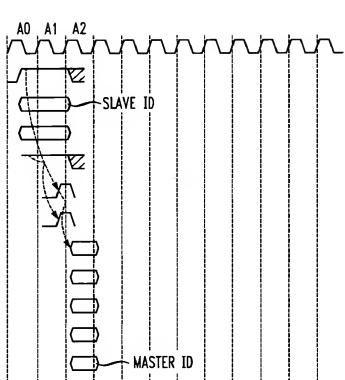


FIG. 5A

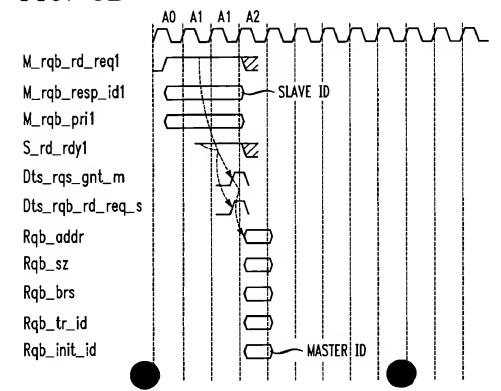
M_rqb_rd_req1
M_rqb_resp_id1
M_rqb_pri1
S_rd_rdy1
Dts_rqs_gnt_m
Dts_rqb_rd_req_s
Rqb_addr
Rqb_sz
Rqb_brs
Rqb_tr_id

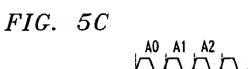


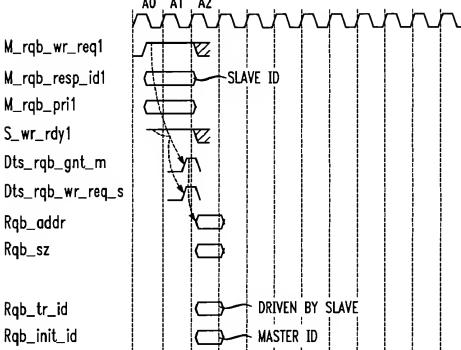
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FIG. 5B

Rqb_init_id

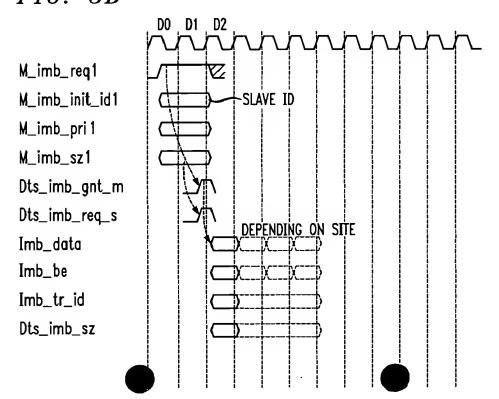


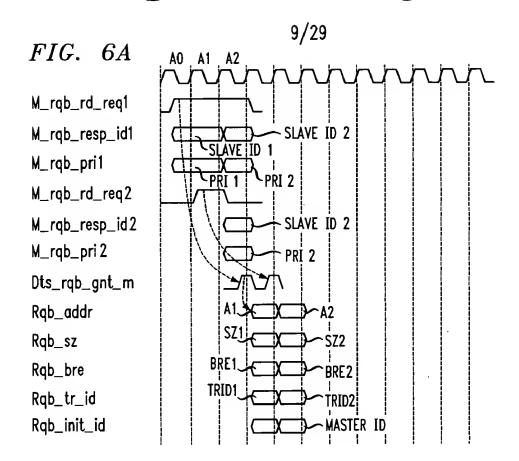


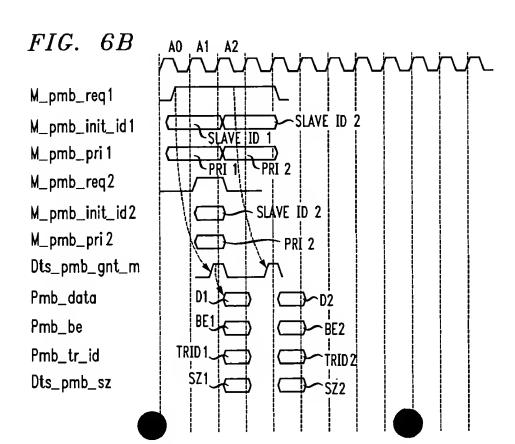


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FIG. 5D







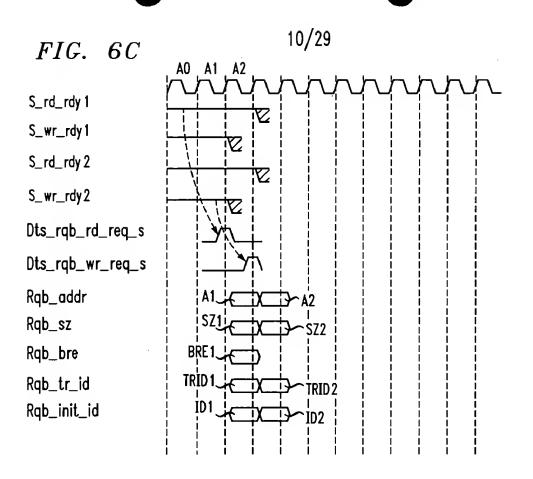
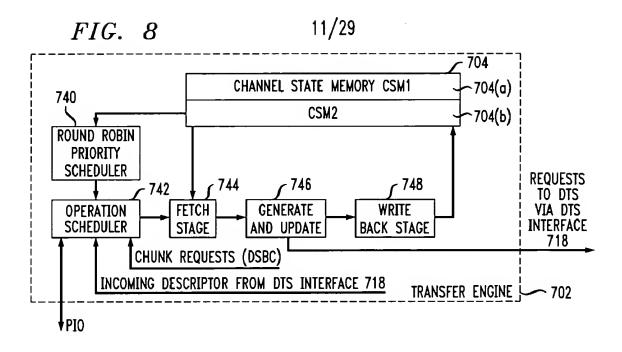


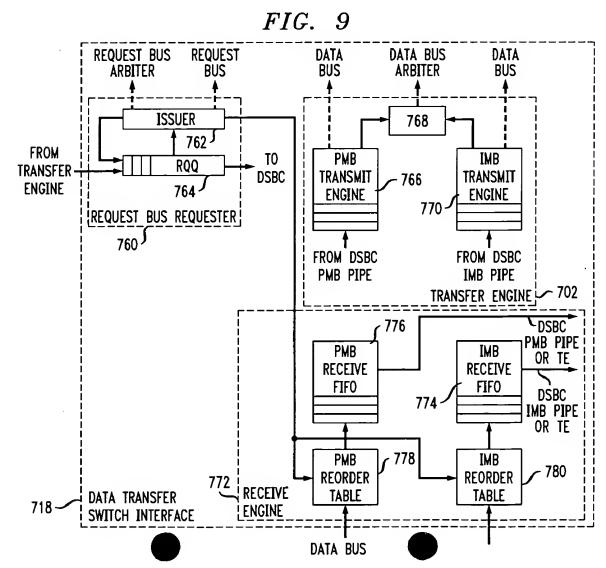
FIG. 7 122 — DATA STREAMER DŤS 718 ~ INTERFACE 716 704 702 CHANNEL STATE TRANSFER INTERNAL **MEMORY ENGINE** FIF0 PIO REQUESTS/DATA BUFFER ~ 714a 706 **MEMORY BUFFER STATE** DATA STREAMER BANK 0 ~714 BUFFER CONTROLLER **MEMORY** BANK 1 708 -714b I/O BUS ARBITER DMA CONTROLLER ~ 138

I/O BUS

710

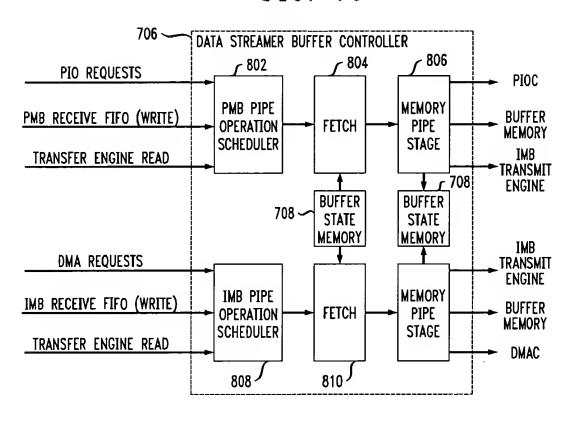
PIOC

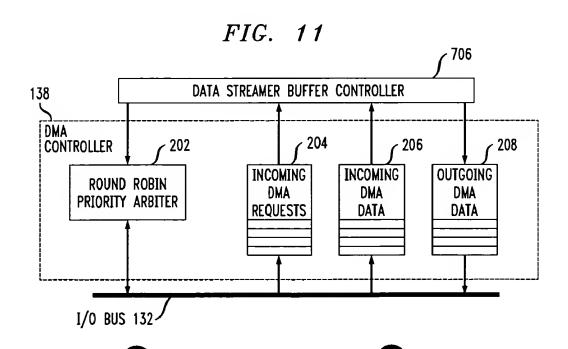




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FIG. 10

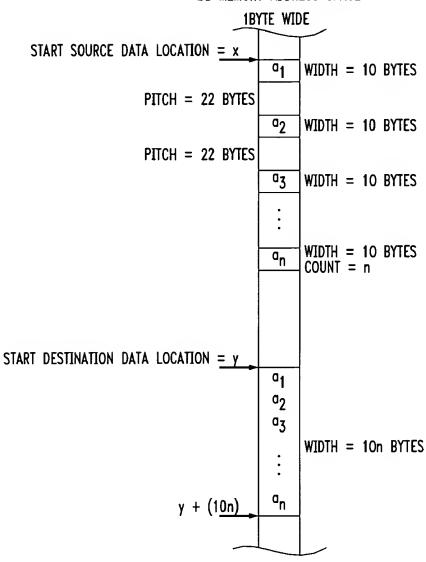




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FIG. 12

4GB MEMORY ADDRESS SPACE



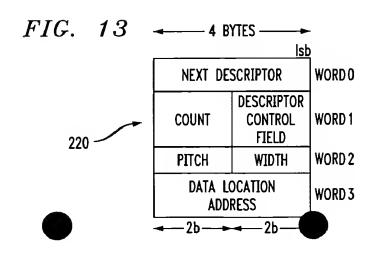
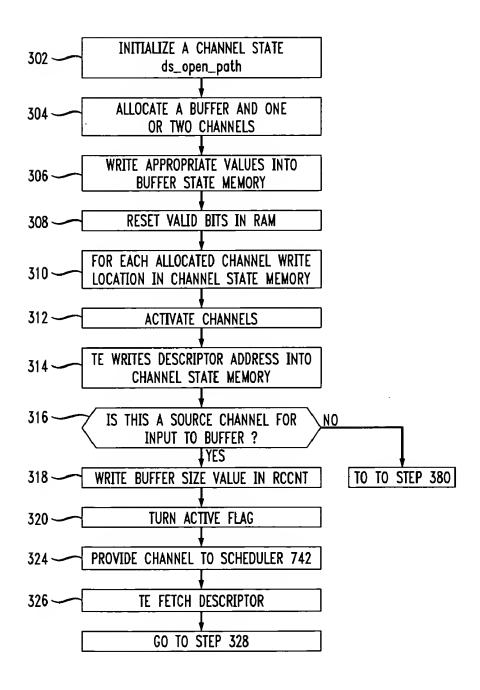


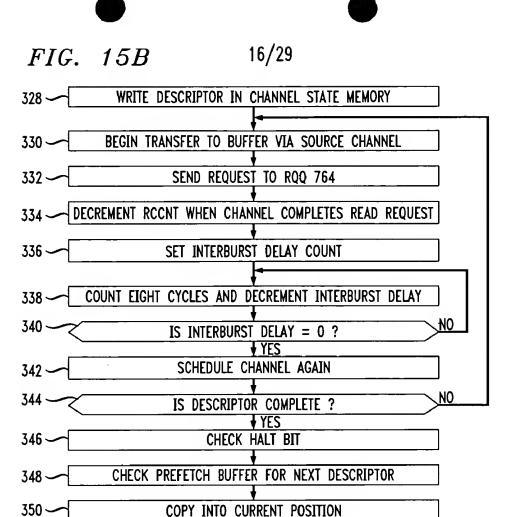
FIG. 14

→ 4 BYTES →		
lsb		
NEXT DESCRIPTOR		
COUNT = k	DESCRIPTOR CONTROL FIELD	
XXXXXX	WIDTH	
DATA LOCATION ADDRESS 1		240
DATA LOCATION ADDRESS 2		
DATA LOCATION ADDRESS 3		
:		
DATA LOCATION ADDRESS k		
2b 2b 2		

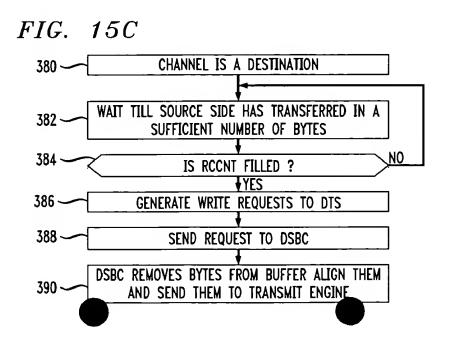
FIG. 15A

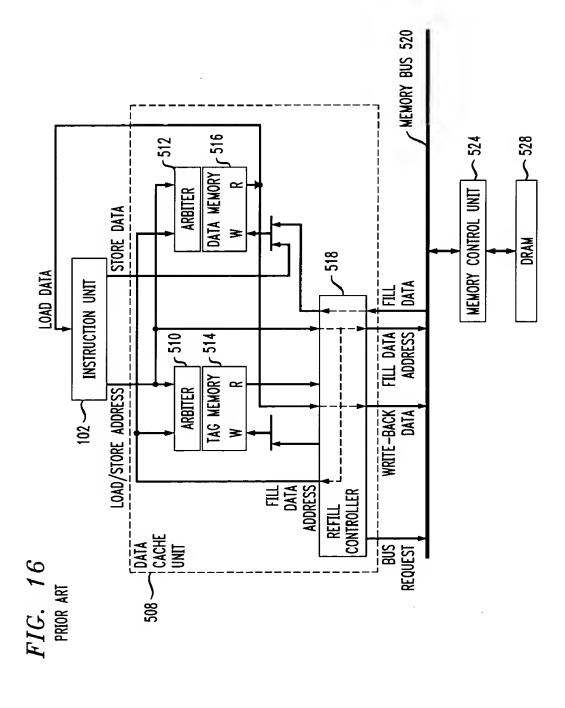


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REPEAT PREFETCH





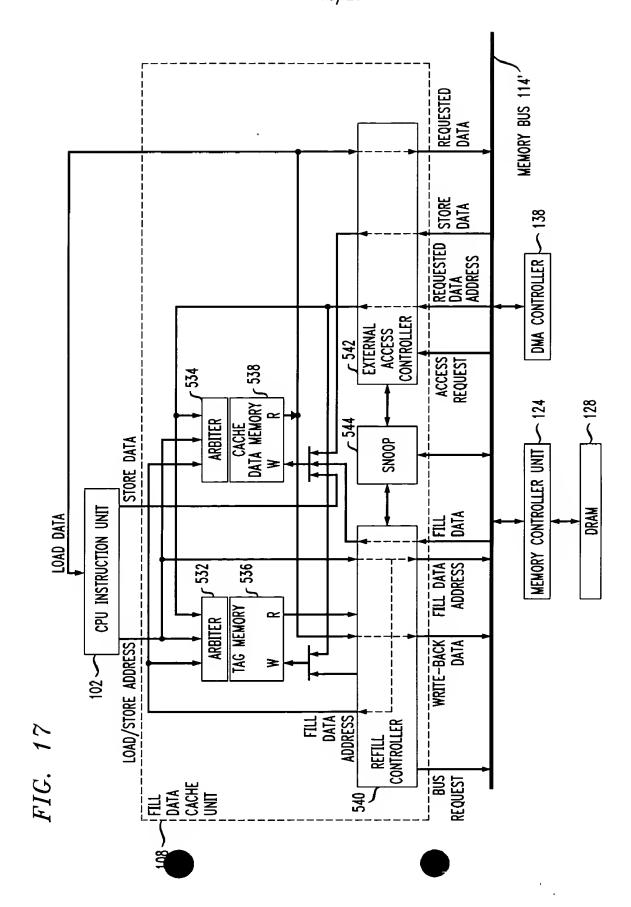


FIG. 18

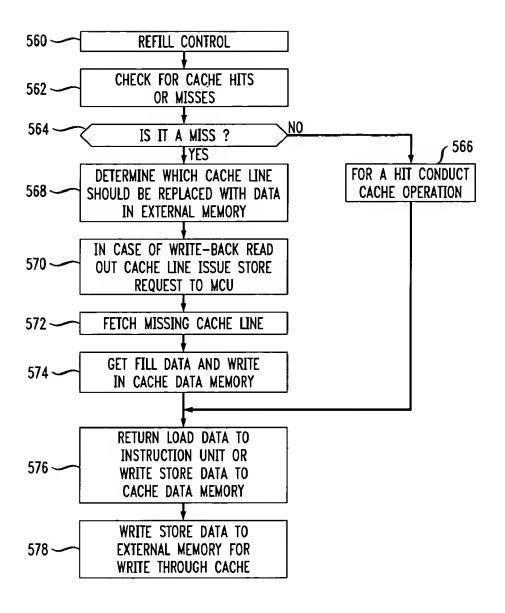
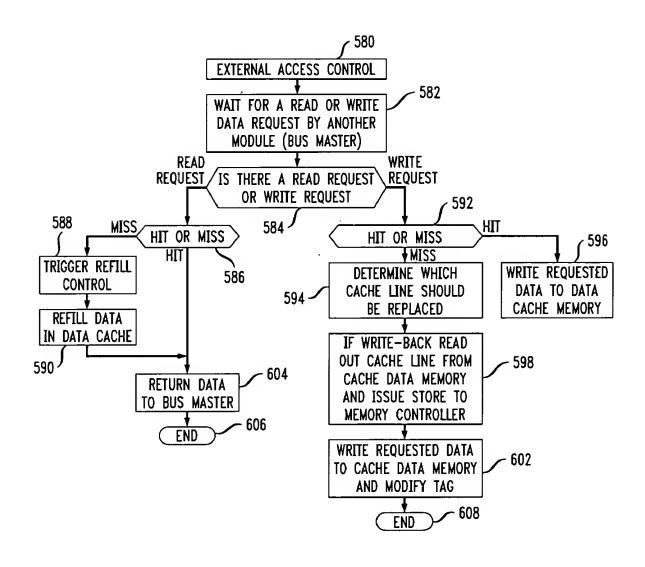


FIG. 19



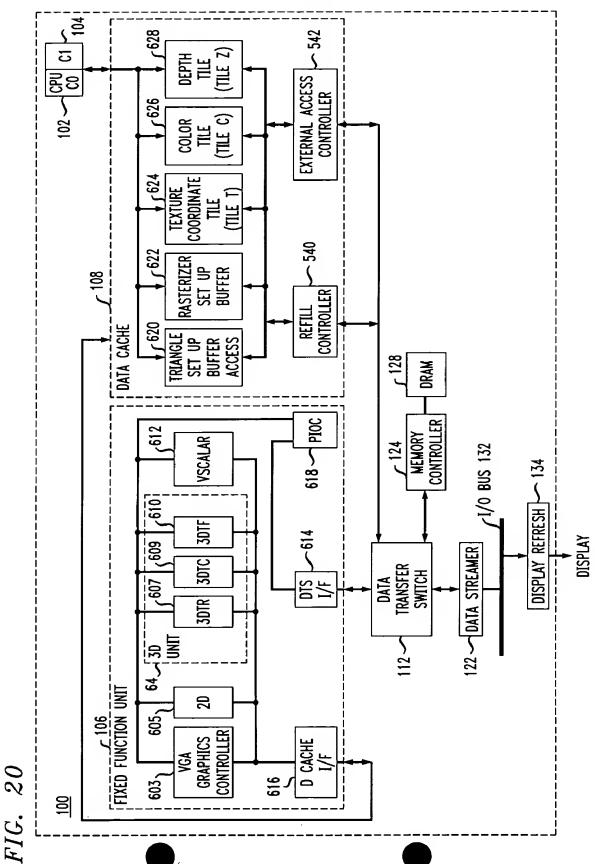


FIG. 21

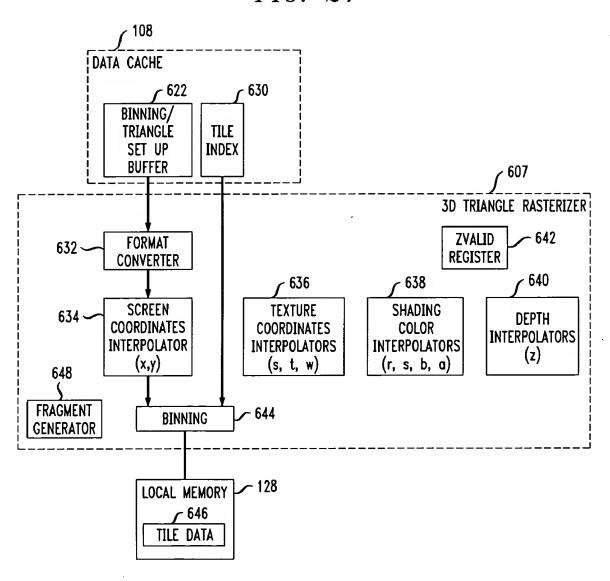


FIG. 22

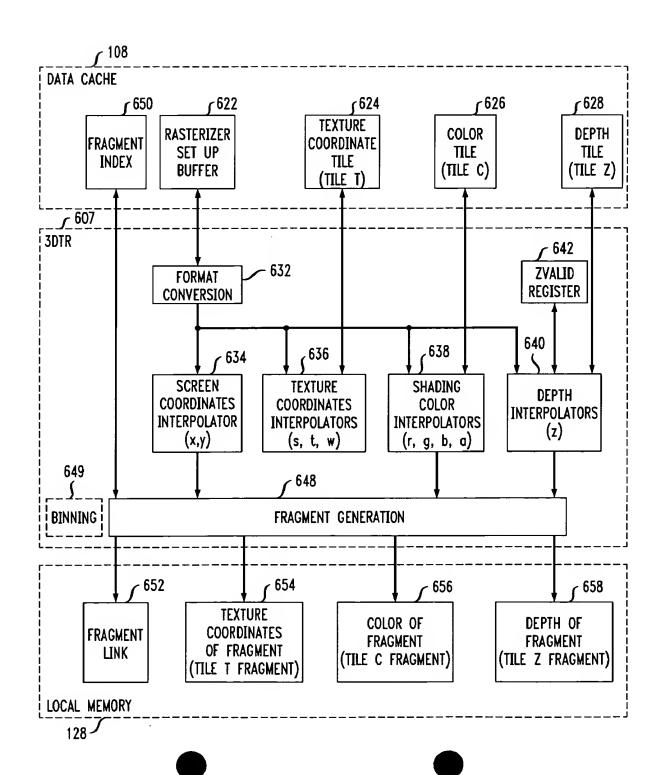


FIG. 23

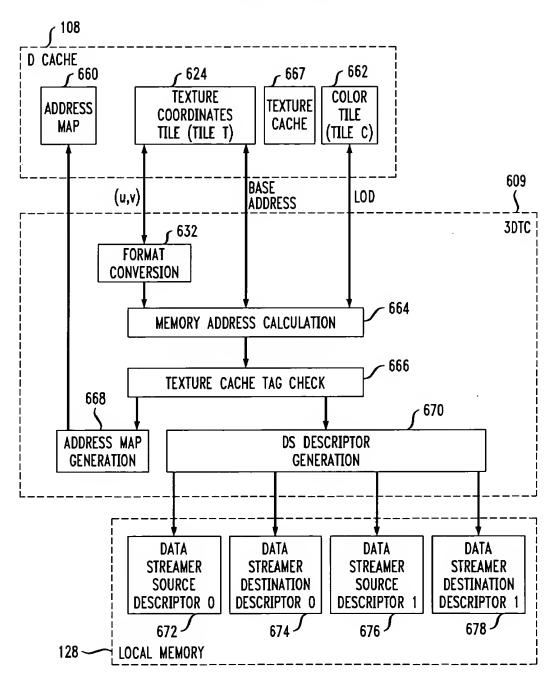
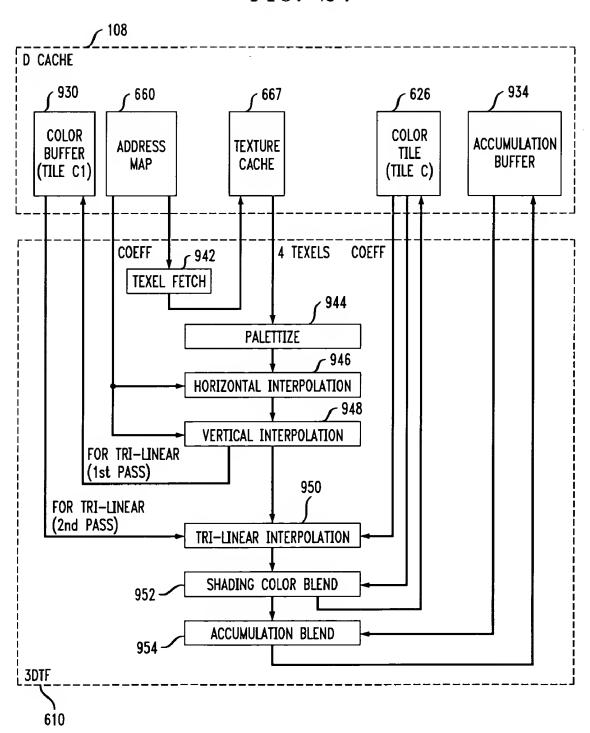
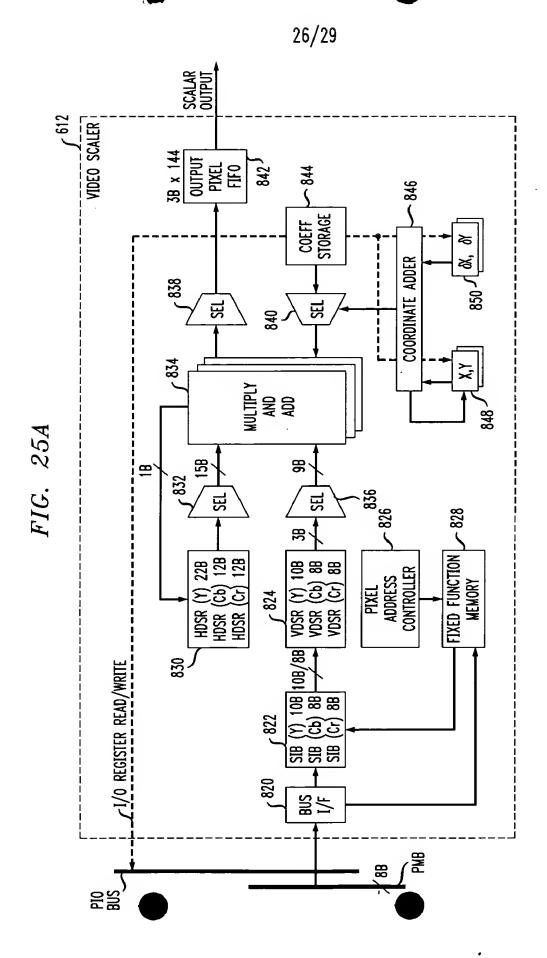


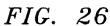
FIG. 24

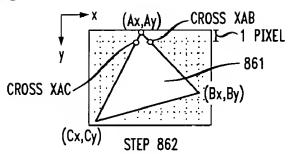


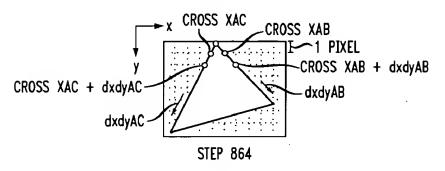


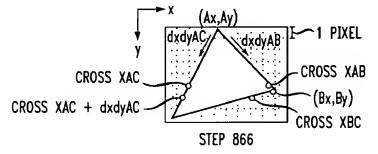
COEFF PIXEL COEFF TEMP PIXEL FIG. 25B 098 J COEFF TEMP PIXEL COEFF TEMP PIXEL 854 **−**856 COEFF MULTIPLY AND ADD TEMP 834 652 PIXEL

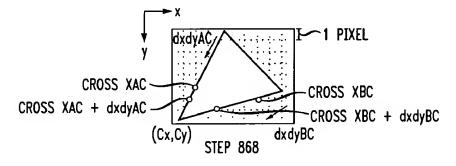
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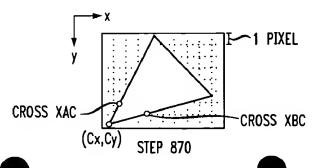












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C)

FIG. 27

